Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A controller for controlling interruption and restarting of data writing to a recording medium, wherein the data written to the recording medium is stored in a buffer memory, the controller comprising:

an encoder connected to the buffer memory, for encoding data which is read data from the buffer memory to generate recording data;

a clock generator connected to the encoder, for generating a system clock and providing the system clock to the encoder to operate the encoder;

a decoder connected to the clock generator, for decoding the data written on the recording medium to generate decoded data; and

a system control circuit connected to the encoder, the clock generator, and the decoder, for deciding whether the encoding of the encoder and the decoding of the decoder are synchronized and starting to write the recording data to the recording medium from the encoder when the encoding of the encoder and the decoding of the decoder are synchronized, subsequent to the interruption of the recording of data,

wherein the clock generator suspends ~~to provide~~ providing the system clock to the encoder until the decoding catches up with the encoding, when the decoding of the decoder is delayed from the encoding of the encoder, generates a first system clock in accordance with the decoding of the decoder, generates a second system clock based on a reference clock having a predetermined frequency, provides the first system clock to the encoder until the encoding of the encoder and the decoding of the decoder are synchronized, and provides the second system clock to the encoder after the encoding and the decoding are synchronized.

2. (Cancelled)

3. (Currently amended) The controller according to claim [[2]] 1, wherein the decoder generates a pit clock based on the decoded data, and the clock generator generates the first system clock based on the pit clock.

4. (Original) The controller according to claim 3, wherein the clock generator includes a phase-locked loop (PLL) circuit connected to the decoder, wherein the PLL circuit generates the first system clock and the second system clock and selectively outputs the first and second system clocks.

5. (Original) The controller according to claim 3, wherein the clock generator includes:

a first PLL circuit connected to the decoder to generate a first system clock;

a second PLL circuit for generating a second system clock based on a reference clock; and

a clock control circuit connected to the first and second PLL circuits, wherein the clock control circuit selectively provides the first and second system clocks to the encoder.

6. (New) A controller for controlling interruption and restarting of data writing to a recording medium, wherein the data written to the recording medium is stored in a buffer memory, the controller comprising:

an encoder connected to the buffer memory, for encoding data which is read data from the buffer memory to generate recording data;

a clock generator connected to the encoder, for generating a system clock and providing the system clock to the encoder to operate the encoder;

a decoder connected to the clock generator, for decoding the data written on the recording medium to generate decoded data; and

a system control circuit connected to the encoder, the clock generator, and the decoder, for deciding whether the encoding of the encoder and the decoding of the decoder are synchronized and starting to write the recording data to the recording medium from the encoder when the encoding of the encoder and the decoding of the decoder are synchronized, subsequent to the interruption of the recording of data,

wherein the clock generator suspends providing the system clock to the encoder until the decoding catches up with the encoding, when the decoding of the decoder is delayed from the encoding of the encoder during synchronization of the encoder and the decoder.

7. (New) The controller according to claim 6, wherein the clock generator generates a first system clock in accordance with the decoding of the decoder, generates a second system clock based on a reference clock having a predetermined frequency, provides the first system clock to the encoder until the encoding of the encoder and the decoding of the decoder are synchronized, and provides the second system clock to the encoder after the encoding and the decoding are synchronized.

8. (New) The controller according to claim 7, wherein the decoder generates a pit clock based on the decoded data, and the clock generator generates the first system clock based on the pit clock.

9. (New) The controller according to claim 8, wherein the clock generator includes a phase-locked loop (PLL) circuit connected to the decoder, wherein the PLL circuit generates the first system clock and the second system clock and selectively outputs the first and second system clocks.

10. (New) The controller according to claim 8, wherein the clock generator includes:

a first PLL circuit connected to the decoder to generate a first system clock;

a second PLL circuit for generating a second system clock based on a reference clock; and

a clock control circuit connected to the first and second PLL circuits, wherein the clock control circuit selectively provides the first and second system clocks to the encoder.

11. (New) A controller for controlling interruption and restarting of data writing to a recording medium, wherein the data written to the recording medium is stored in a buffer memory, and the controller controls the interruption of the data writing to the recording medium when the buffer memory is in a state in which buffer underrun may occur and controls the restarting of the data writing to the recording medium when the buffer memory is in a state in which buffer underrun is no longer likely to occur, the controller comprising:

an encoder connected to the buffer memory, for encoding data which is read data from the buffer memory to generate recording data;

a clock generator connected to the encoder, for generating a system clock and providing the system clock to the encoder to operate the encoder;

a decoder connected to the clock generator, for decoding the data written on the recording medium to generate decoded data; and

a system control circuit connected to the encoder, the clock generator, and the decoder, for deciding whether the encoding of the encoder and the decoding of the decoder are synchronized and starting to write the recording data to the recording medium from the encoder when the encoding of the encoder and the decoding of the decoder are synchronized, subsequent to the interruption of the recording of data,

wherein, the clock generator suspends providing the system clock to the encoder until the decoding catches up with the encoding, when the decoding of the decoder is delayed from the encoding of the encoder.

12. (New) The controller according to claim 11, wherein the clock generator generates a first system clock in accordance with the decoding of the decoder, generates a second

system clock based on a reference clock having a predetermined frequency, provides the first system clock to the encoder until the encoding of the encoder and the decoding of the decoder are synchronized, and provides the second system clock to the encoder after the encoding and the decoding are synchronized.

13. (New) The controller according to claim 12, wherein the decoder generates a pit clock based on the decoded data, and the clock generator generates the first system clock based on the pit clock.

14. (New) The controller according to claim 13, wherein the clock generator includes a phase-locked loop (PLL) circuit connected to the decoder, wherein the PLL circuit generates the first system clock and the second system clock and selectively outputs the first and second system clocks.

15. (New) The controller according to claim 13, wherein the clock generator includes:

a first PLL circuit connected to the decoder to generate a first system clock;

a second PLL circuit for generating a second system clock based on a reference clock; and

a clock control circuit connected to the first and second PLL circuits, wherein the clock control circuit selectively provides the first and second system clocks to the encoder.